IN THE CLAIMS

Please cancel claims 2 and 14.

1. (Currently Amended) A machine-implemented method comprising:

multiplying matrix [A] by matrix [x] to obtain matrix [y];

wherein said matrix [x] is a matrix of inputs, said matrix [y] is a matrix of outputs, and said matrix [A] is a matrix of predetermined values and multiplication operations;

wherein said multiplication operations within said [A] are paired; [[and]]

wherein the method is implemented using machine-implemented Packed Multiply and Add (PMADDWD) instructions;

wherein said matrix [A] is factored into a butterfly matrix [B], a shuffle matrix [S], and a multiplication matrix [M]; and

wherein multiplication operations within said multiplication matrix [M] are grouped for simultaneous execution.

2. (Canceled)

3. (Original) The method as in claim 1, wherein at least one n-point discrete cosine transform (DCT) is performed.

4. (Original) The method as in claim 3, wherein multimedia compression is performed.

5. (Original) The method as in claim 3, wherein at least one shape adaptive discrete cosine transform (SA-DCT) is performed.

6. (Original) The method as in claim 1, wherein at least one n-point inverse discrete cosine transform (IDCT) is performed.

7. (Original) The method as in claim 6, wherein multimedia decompression is performed.

8. (Currently Amended) The method as in claim 6, wherein at least one shape adaptive inverse discrete cosine transform (SA-IDCT) is performed.

9. (Original) The method as in claim 1, implemented using single instruction multiple data (SIMD) operations.

10. (Previously Presented) The method as in claim 9, implemented using Multimedia Extension (MMX) operations.

11. (Canceled)

12. (Previously Presented) The method as in claim 1, implemented using at least one of very large scale integration (VLSI) implementation, single processor implementation, and vector processing.

13. (Currently Amended) A machine readable storage medium having executable instructions which, when executed by a machine, cause said machine to perform operations comprising:

multiplying matrix [A] by matrix [x] to obtain matrix [y];

wherein said matrix [x] is a matrix of inputs, said matrix [y] is a matrix of outputs, and said matrix [A] is a matrix of predetermined values and multiplication operations;

wherein said multiplication operations within said matrix [A] are paired; and

wherein the operations are implemented using machine-implemented Packed Multiply and Add (PMADDWD) instructions;

wherein said matrix [A] is factored into butterfly matrix [B], shuffle matrix [S], and multiplication matrix [M]; and

wherein multiplication operations within said multiplication matrix [M] are grouped for simultaneous execution.

14. (Canceled)

15. (Currently Amended) The machine readable storage medium as in claim 13, wherein at least one n-point discrete cosine transform (DCT) is performed.

16. (Original) The machine readable storage medium as in claim 15, wherein multimedia compression is performed.

17. (Currently Amended) The machine readable storage medium as in claim 15, wherein at least one shape adaptive discrete cosine transform (SA-DCT) is performed.

18. (Currently Amended) The machine readable storage medium as in claim 13, wherein at least one n-point inverse discrete cosine transform (IDCT) is performed.

19. (Original) The machine readable storage medium as in claim 18, wherein multimedia decompression is performed.

20. (Currently Amended) The machine readable storage medium as in claim 18, wherein at least one shape adaptive discrete cosine transform (SA-IDCT) is performed.

21. (Currently Amended) The machine readable storage medium as in claim 13, implemented using single instruction multiple data (SIMD) operations.

22. (Previously Presented) The machine readable storage medium as in claim 21, implemented using Multimedia Extension (MMX) operations.

23. (Canceled)

24. (Currently Amended) The machine readable storage medium as in claim 13, implemented using at least one of very large scale integration (VLSI) implementation, single processor implementation, vector processing.

25. (Currently Amended) A method comprising performing an n-point discrete cosine transform (DCT) or an n-point inverse discrete cosine transform (IDCT) wherein multiplication operations and addition operations within said n-point DCT and said n-point IDCT are paired, wherein the method is implemented using machine-implemented Packed Multiply and Add (PMADDWD) instructions, and wherein the multiplication operations are grouped within a multiplication matrix for simultaneous execution.

26. (Original) The method as in claim 25, further comprising performing SA-DCT or SA-IDCT.

27. (Original) The method as in claim 25, implemented using instructions that can execute multiple operations in parallel.

28. (Previously Presented) The method as in claim 27, said instructions being at least one of Multimedia Extension (MMX) operations and Streaming SIMD Extensions.